MICROCOMPUTER AND COMPUTER SYSTEM

FIELD OF THE INVENTION

The present invention relates to a microcomputer and a computer system. More particularly, this invention relates to a one-chip microcomputer, for example used in vehicles, and having a stop releasing function for prime oscillation. This invention also relates to a computer system that uses such a microcomputer.

BACKGROUND OF THE INVENTION

Generally, there is a state known as deadlock as an abnormal operation in the microcomputer. During deadlock, prime oscillation is stopped unexpectedly and the operation mode shifted from run to stop due to the generation of broken data in some latch circuits. The broken data is generated because of sudden changes in supply voltage or influence of external noise etc. The CPU has no control on the occurrence of the deadlock. One-chip microcomputer are used in vehicles for controlling electronic equipment. It is very important to provide a fail safe function in such microcomputers to prevent generation of a deadlock.

Conventionally, there is known an external reset function to realize the fail safe function. In this external reset function, a reset signal is input into a reset terminal

of the microcomputer from outside and the CPU is reset to initial state. There is also know an external interrupt function or non-maskable interrupt (NMI) function to realize the fail safe function. In this external interrupt function or non-maskable interrupt (NMI) function, an interrupt requesting signal is input into an external interrupt (INT) terminal or a non-maskable terminal of the microcomputer from outside. As a consequence, an interrupt occurs, and an interrupt processing is executed.

However, in the external reset function, since internal register value is initialized because of the reset, there is a problem that the data is lost. There may be thought of a method that does not initialize the needful resources even if the reset signal is input. However, such method is not practical because needful resources that should not be initialized differ depending upon how and where the microcomputer is being used.

Moreover, in the external interrupt function, only when it is transited to state of stop after permission of external interrupt is set by software, state of stop is released by means of input of the interrupt requesting signal. Therefore, when it is transited to state of stop before setting of permission of interrupt, state of stop cannot be released. In addition, in the non-maskable interrupt function, there is a problem that since interrupt processing

is executed unconditionally in not only state of stop but also normal state of run, unnecessary code is executed by execution of interrupt processing in normal state of run.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a microcomputer having a fail safe function such that state of stop can be released by only hardware without intervention of software factors and thereby the deadlock is avoided.

The microcomputer according to one aspect of the present invention comprises an oscillation circuit which oscillates and outputs an oscillation signal and stops the oscillation during a period in which it receives an oscillation stop signal; a wakeup terminal that receives from outside a wakeup signal of a predetermined cycle; and a clock control circuit which receives the wakeup signal, outputs the oscillation stop signal, and stops output of the oscillation stop signal based on the wakeup signal.

In normal state of run, the oscillation signal is supplied from the oscillation circuit to the clock control circuit. The clock control circuit generates a main clock signal based on the oscillation signal. Moreover, in normal state of run, the clock control circuit ignores the wakeup signal in order not to affect its operation state.

On the other hand, in state of stop, the clock control

circuit supplies an oscillation stop signal to the oscillation circuit, thereby the oscillation circuit stops oscillation. In this state, when the wakeup signal is input into the clock control circuit, the clock control circuit forces the oscillation stop signal to release. When the oscillation stop signal is released, the oscillation circuit resumes oscillation. The microcomputer becomes normal state of run through state of oscillation stability wait.

Moreover, the computer system according to another aspect of the present invention comprises the above-mentioned microcomputer and a wakeup signal supplying unit that supplies the wakeup signal on predetermined cycle constantly.

Other objects and features of this invention will become apparent from the following description with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing a main section of the microcomputer of the embodiment of the present invention;

Fig. 2 is a state transition diagram for explaining the transition of operation state of the microcomputer of the embodiment of the present invention;

Fig. 3 is a block diagram showing a main section of the microcomputer of a first embodiment of the present

invention;

Fig. 4 is a state transition diagram for explaining the transition of operation state of the microcomputer of the first embodiment;

Fig. 5 is a block diagram showing a main section of the microcomputer of a second embodiment of the present invention;

Fig. 6 is a state transition diagram for explaining the transition of operation state of the microcomputer of the second embodiment;

Fig. 7 is a block diagram showing a main section of the microcomputer of a third embodiment of the present invention; and

Fig. 8 is a state transition diagram for explaining the transition of operation state of the microcomputer of the third embodiment.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Embodiments of a microcomputer and a computer system according to the present invention will be described below in detail with reference to the accompanying drawings.

Fig. 1 is a block diagram showing required sections of the microcomputer according to an embodiment of the present invention. Fig. 2 is a state transition diagram of the microcomputer. The microcomputer has the wakeup

terminal 11 to which the wakeup signal 21 is supplied from outside on suitable cycle. The wakeup signal 21 is then supplied to the clock control circuit 12. A not shown oscillator is connected with the oscillation circuit 13 through oscillation terminals 14, 15 shown by X0, X1.

In normal state of run, the oscillation signal (HCLK) 22 is supplied from the oscillation circuit 13 to the clock control circuit 12. The clock control circuit 12 generates the main clock signal 23 based on the oscillation signal 22 to supply the signal 23 to various circuits (not shown) in the microcomputer. Moreover, in normal state of run, the clock control circuit 12 ignores the wakeup signal 21 in order not to affect its operation state.

In state of stop, the clock control circuit 12 supplies the oscillation stop signal 26 (KLHI) to the oscillation circuit 13, thereby the oscillation circuit 13 stops oscillation. In this state, when the wakeup signal 21 is input into the clock control circuit 12, the clock control circuit 12 forces the oscillation stop signal 26 to release. When the oscillation stop signal 26 is released, the oscillation circuit 13 resumes oscillation. The microcomputer becomes normal state of run through state of oscillation stability wait.

Moreover, the microcomputer executes interrupt processing when the interrupt requesting signal 24 is

supplied to the interrupt control circuit 17 from outside through the external interrupt (INT) terminal 16. In addition, the microcomputer returns to initial state when the reset signal 25 is supplied from outside through the reset (RSTX) terminal 18.

Fig. 3 is a block diagram showing only required sections of the microcomputer according to a first embodiment of the present embodiment. Fig. 4 is a state transition diagram of the microcomputer according to the first embodiment. The microcomputer 1 shown in Fig. 3 has the same configuration as the microcomputer shown in Fig. 1, therefore, repetition of explanation will be omitted. The oscillator 2 is connected with oscillation terminals 14, 15. The oscillator 2 is a crystal oscillator whose oscillation frequency is 4 MHz, for example. The wakeup signal supplying unit 3 is connected with the wakeup terminal 11.

The wakeup signal supplying unit 3 always generates H level signal whose potential level is relatively high by constant cycle, for example, 4 sec. to supply it to the wakeup terminal 11. The signal input from the wakeup terminal 11 is supplied to the clock control circuit 12 as the wakeup signal 21. The oscillator 2 and the wakeup signal supplying unit 3 are arranged out of the microcomputer 1. The external interrupt terminal, the interrupt control circuit and the reset terminal are not shown and omitted.

The clock control circuit 12 ignores the input the wakeup signal 21 in normal state of run, that is, in state in which the oscillation signal 22 is supplied from the oscillation circuit 13. Thus, even if the wakeup signal 21 is input into the clock control circuit 12 in normal state of run, state of the microcomputer 1 dose not change, and it is not transited to state of stop. When the microcomputer 1 transits to state of stop by cause such as occurrence of data illegibility in some latch circuits, the clock control circuit 12 supplies the oscillation stop signal 26 to the oscillation circuit 13. By input of the oscillation stop signal 26, the oscillation circuit 13 stops oscillation, and the microcomputer 1 transits to state of stop. At this time, internal register value is held as it is, thereby state of Input/Output is stored.

At this time, if it is transited to state of stop with external interrupt request prohibited by software, interrupt does not occurred even if the interrupt request signal is input from the external interrupt terminal not shown to the microcomputer 1. In other words, in this case, state of stop cannot be released by means of external interrupt. However, in this embodiment, the clock control circuit 12 comprises function that the circuit 12 forces the oscillation stop signal 26 to release when the wakeup signal 21 is input at the time of state of stop.

Therefore, the oscillation stop signal 26 is released forcedly, and the oscillation circuit 13 resumes oscillation. After resumption of oscillation, the microcomputer 1 returns to normal state of run through state of oscillation stability wait and resumes processing from the following instruction of the instruction executed just before state of stop using register value which has been held when stopping.

According to the first embodiment, since the clock control circuit 12 forces the oscillation stop signal 26 to release based on input of the wakeup signal 21 in state of stop, the oscillation circuit 13 resumes oscillation speedily even if it is transited from normal state of run to state of stop with external interrupt request prohibited. Therefore, since state of stop of prime oscillation can be released by only hardware without software, state of deadlock can be avoided.

Fig. 5 is a block diagram showing a main section of the microcomputer according to a second embodiment of the present embodiment. Fig. 6 is a state transition diagram of the microcomputer according to the second embodiment. The second embodiment differs from the first embodiment in that a microcomputer 101 according to the second embodiment is constituted so that the signal of H level supplied from the wakeup signal supplying unit 3 is supplied to the clock control circuit 12 as the wakeup signal 21 and also to the

interrupt control circuit 17 through the external interrupt terminal 16 as the interrupt requesting signal 24. Moreover, the same reference letters are added with respect to the same constitution as the first embodiment and description about them is omitted.

By such constitution, when it is transited from normal state of run to state of stop after permission of external interrupt request by software, the oscillation stop signal 26 is released forcedly by input of the wakeup signal 21 and the oscillation circuit 13 resumes oscillation. At this time, since the interrupt requesting signal 24 is input into the interrupt control circuit 17, for example, leading edge of the interrupt requesting signal 24 is detected, thereby interrupt is created, and then after state of oscillation stability wait the CPU not shown executes interrupt processing.

When it is transited to state of stop with external interrupt request prohibited by software, interrupt does not occurred even if the interrupt request signal 24 is input into the interrupt control circuit 17 at the same time that prime oscillation is resumed. Therefore, in this case, the microcomputer 101 returns to normal state of run like the first embodiment. In the second embodiment, when external interrupt request is permitted in normal state of run, interrupt occur by means of the signal input as the interrupt

requesting signal 24 from the external interrupt terminal 16.

According to the second embodiment, since the clock control circuit 12 forces the oscillation stop signal 26 to release based on input of the wakeup signal 21 in state of stop, the oscillation circuit 13 resumes oscillation speedily even if it is transited from normal state of run to state of stop. At this time, since the interrupt request signal 24 is supplied to the interrupt control circuit 17, if prime oscillation is resumed from state that it is transited to state of stop after permission of external interrupt request, the microcomputer 101 executes interrupt processing. Therefore, since state of stop of prime oscillation can be released and interrupt processing can be executed by only hardware without software, state of deadlock can be avoided.

Fig. 7 is a block diagram showing a main section of the microcomputer according to a third embodiment of the present embodiment. Fig. 8 is a state transition diagram of the microcomputer according to the third embodiment. The third embodiment differs from the first embodiment in that a microcomputer 201 according to the third embodiment comprises an address generating circuit 19 outputting predetermined address and is constituted so that the signal of H level supplied from the wakeup signal supplying unit

3 is supplied to the clock control circuit 12 as the wakeup signal 21 and also to the address generating circuit 19. Moreover, the same reference letters are added with respect to the same constitution as the first embodiment and description about them is omitted.

By such constitution, when it is transited from normal state of run to state of stop with external interrupt request prohibited, the oscillation stop signal 26 is released forcedly by input of the wakeup signal 21 and the oscillation circuit 13 resumes oscillation. The microcomputer 201 is transited to state of oscillation stability wait. Moreover, since the wakeup signal 21 is input into the address generating circuit 19 as a trigger signal for generating address at the same time that prime oscillation is resumed, the address generating circuit 19 outputs specific address set beforehand, for example, FFA000h. Then, after state of oscillation stability wait, the CPU not shown executes processing from instruction in memory space of FFA000h.

According to the third embodiment, since the clock control circuit 12 forces the oscillation stop signal 26 to release based on input of the wakeup signal 21 in state of stop, the oscillation circuit 13 resumes oscillation speedily even if it is transited from normal state of run to state of stop with external interrupt request prohibited. At this time, since specific address is output from the

address generating circuit 19, the microcomputer 201 executes processing from instruction in memory space corresponding to its address. Therefore, since state of stop of prime oscillation can be released by only hardware without software and processing can be executed from instruction in memory space of specific address, state of deadlock can be avoided.

It is to be understood that the invention is not limited to the specific embodiments thereof and various changes and modifications may be made in the invention. For example, constitution in which an automatic start type watch dog timer which always operates at the time that the oscillation circuit 13 is oscillating is contained in the microcomputer as fail safe function for runaway of program after release of state of stop may be possible. Moreover, the present invention may be applied to not only one-chip microcomputer but also a microcomputer carried on the same LSI package, one-board microcomputer and system microcomputer. Furthermore, in the third embodiment, the address generating circuit 19 may be arranged outside the microcomputer 201.

According to the present invention, state of stop of prime oscillation can be released by only hardware without software. Therefore, a microcomputer having a fail safe function that prevents generation of deadlock can be obtained.

Although the invention has been described with respect to a specific embodiment for a complete and clear disclosure, the appended claims are not to be thus limited but are to be construed as embodying all modifications and alternative constructions that may occur to one skilled in the art which fairly fall within the basic teaching herein set forth.